forming first and second semiconductor line, each end of the silicon lines contacting one of the source and the drain;

forming an etch stop layer on an exposed side surface of each of the first and second semiconductor lines;

epitaxially growing first and second semiconductor layers on each etch stop layer;

etching away the first and second semiconductor lines and the etch stop layers;

filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and the drain with an oxide fill; and

etching a portion of the oxide fill to form an area that defines a gate, wherein the area that defines the gate is substantially centered between and substantially parallel to the source and the drain.

19. (Amended) The method as recited in claim 14, further comprising the steps of:

implanting a portion of the epitaxially grown silicon layers between the gate and the source; and

implanting a portion of the epitaxially grown silicon layers between the gate and the drain.

20. (Amended) The method as recited in claim 19, wherein the implanting step is in the range of 10 to 45 degrees relative to a vector perpendicular to a top surface of the epitaxially grown silicon layers.

21. (Amended) The method as recited in step 20, wherein the implants are done in a series at approximately 90 degrees relative to each other.

Add the following new claims:

24. A method of forming an FET, comprising:

forming a first semiconductor layer having first and second ends and a central region that is thinner than said first and second ends, said central region having first and second side surfaces;

epitaxially growing a semiconductor channel region on at least one of said first and second side surfaces of said central region of said first semiconductor layer;
removing said central region of said first semiconductor layer;
forming a dielectric layer on exposed surfaces of said semiconductor channel region; and
forming a gate electrode on said dielectric layer.

25. The method of claim 24, wherein said semiconductor channel region is formed of a combination of Group IV elements.

26. The method of claim 24, wherein said semiconductor channel region is formed of an alloy of silicon and Group IV element.

27. The method of claim 24, wherein said semiconductor channel region is formed of a material selected from the group consisting of silicon, silicon-germanium, and silicon-germanium-carbon.

28. The method of claim 27, wherein said step of removing said first semiconductor layer does not appreciably remove said semiconductor channel region.

29. The method of claim 28, wherein an etch stop is epitaxially grown between said first semiconductor layer and said semiconductor channel region.

30. The method of claim 24, wherein said gate electrode is formed of a material selected from the group consisting of polysilicon, silicon-germanium, refractory metals, Ir, Al, Ru, Pt, and titanium nitride.

Remarks

Applicants respectfully request that the present amendment be entered, and that the subject US patent application be passed to issuance in view thereof.